

PH8230

N-channel enhancement mode field-effect transistor

Rev. 01 — 23 June 2003

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect power transistor in a SOT669 (LFAK) package.

Product availability:

PH8230 in SOT669 (LFAK).

1.2 Features

- Low thermal resistance
- Low gate drive current
- SO8 equivalent area footprint
- Low on-state resistance.

1.3 Applications

- DC-to-DC converters
- Portable appliances
- Switched mode power supplies
- Notebook computers.

1.4 Quick reference data

- $V_{DS} \leq 30 \text{ V}$
- $P_{tot} \leq 50 \text{ W}$
- $I_D \leq 30 \text{ A}$
- $R_{DSon} \leq 8.2 \text{ m}\Omega$

2. Pinning information

Table 1: Pinning - SOT669 (LFAK), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)		
4	gate (g)		
mb	drain (d)		

SOT669 (LFAK)



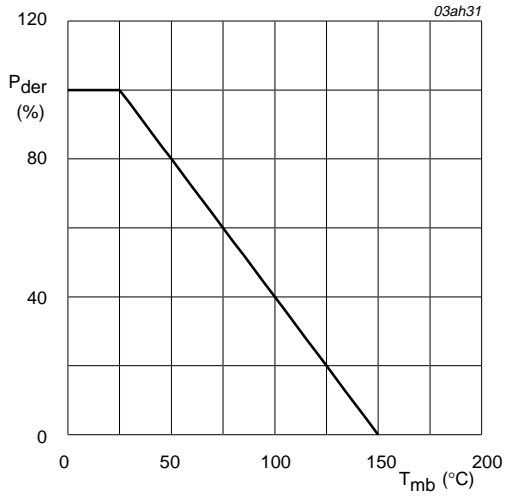
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3. Limiting values

Table 2: Limiting values

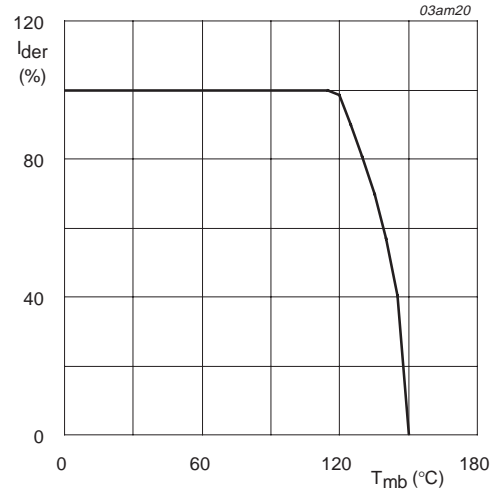
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25$ to 150 °C	-	30	V
V_{GS}	gate-source voltage (DC)		-	± 20	V
I_D	drain current (DC)	$T_{mb} = 25$ °C; $V_{GS} = 10$ V	-	30	A
I_{DM}	peak drain current	$T_{mb} = 25$ °C; pulsed; $t_p \leq 10$ μ s	-	120	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C	-	50	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{mb} = 25$ °C	-	30	A
I_{SM}	peak source (diode forward) current	$T_{mb} = 25$ °C; pulsed; $t_p \leq 10$ μ s	-	120	A



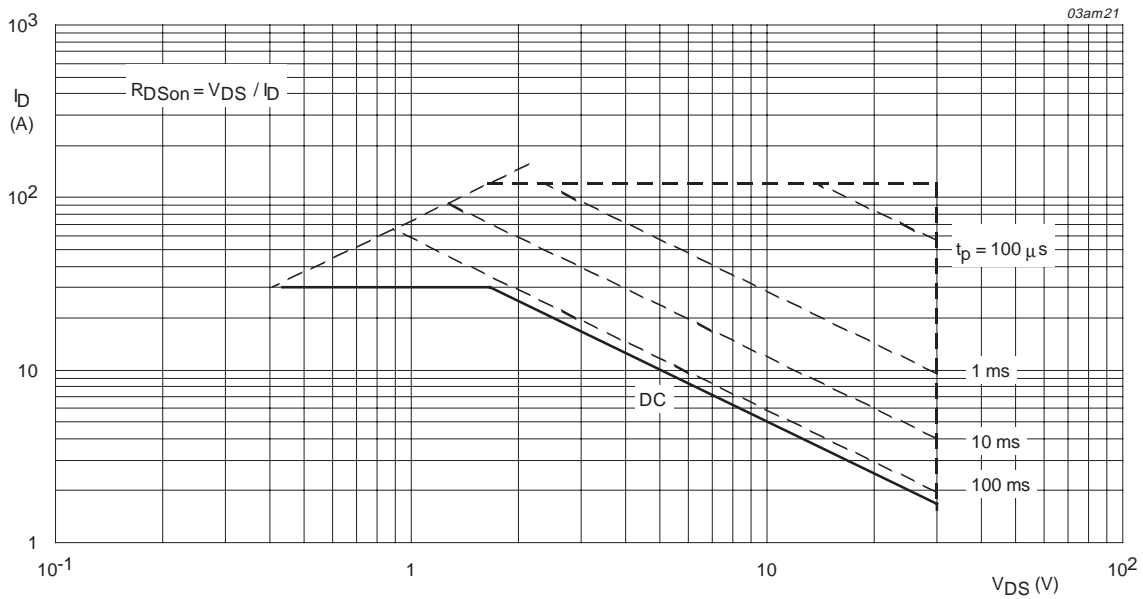
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

4. Thermal characteristics

Table 3: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	-	2.5	K/W

4.1 Transient thermal impedance

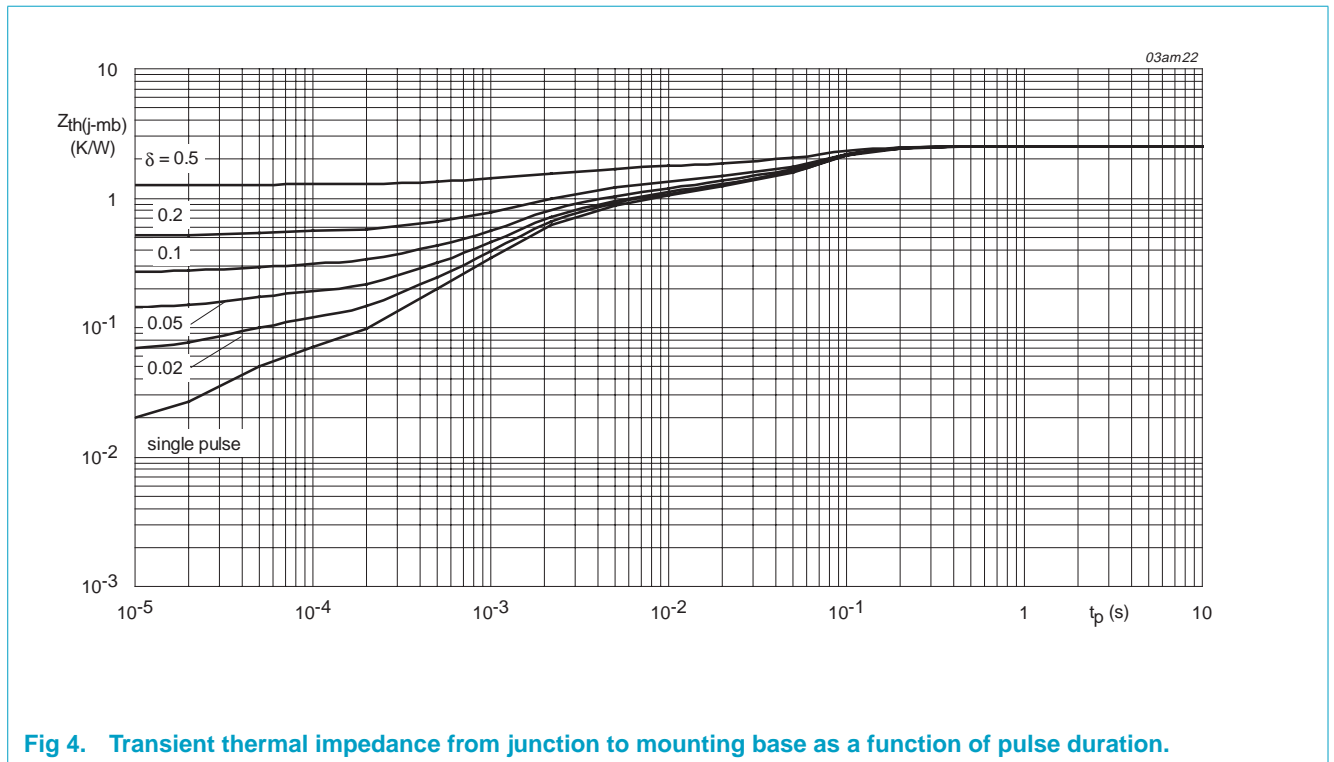


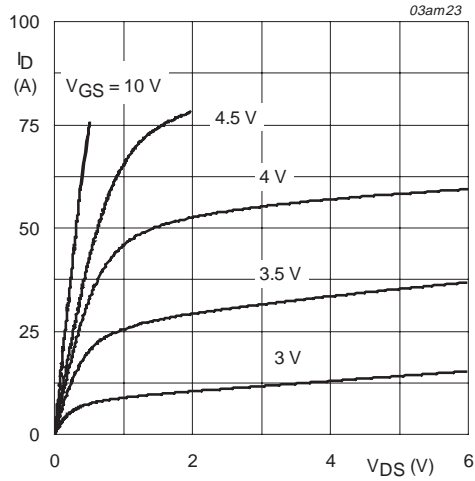
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

5. Characteristics

Table 4: Characteristics

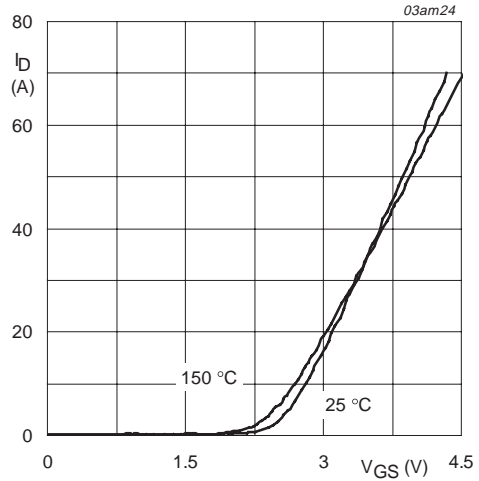
$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\text{ mA}; V_{GS} = 0\text{ V}$	30	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}; V_{DS} = V_{GS}$	1	1.75	2.5	V
I_{DSS}	drain-source leakage current	$V_{DS} = 30\text{ V}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	0.06	1	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 16\text{ V}; V_{DS} = 0\text{ V}$	-	0.9	10	μA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 15\text{ A}$	-	6.3	8.2	$\text{m}\Omega$
		$V_{GS} = 4.5\text{ V}; I_D = 15\text{ A}$	-	10.5	15.3	$\mu\Omega$
Dynamic characteristics						
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 15\text{ A}$	27	45	-	S
$Q_{g(tot)}$	total gate charge	$I_D = 30\text{ A}; V_{DD} = 10\text{ V}; V_{GS} = 10\text{ V}$	-	22	-	nC
Q_{gs}	gate-source charge		-	5	-	nC
Q_{gd}	gate-drain (Miller) charge		-	5	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 10\text{ V}; f = 1\text{ MHz}$	-	1500	-	pF
C_{oss}	output capacitance		-	400	-	pF
C_{riss}	reverse transfer capacitance		-	220	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 10\text{ V}; I_D = 15\text{ A}; V_{GS} = 10\text{ V}; R_G = 4.7\text{ }\Omega$	-	15	-	ns
t_r	rise time		-	55	-	ns
$t_{d(off)}$	turn-off delay time		-	48	-	ns
t_f	fall time		-	11	-	ns
Source-drain (reverse) diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 30\text{ A}; V_{GS} = 0\text{ V}$	-	0.85	1.11	V
t_{rr}	reverse recovery time	$I_S = 30\text{ A}; dI_S/dt = -50\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}$	-	60	-	ns



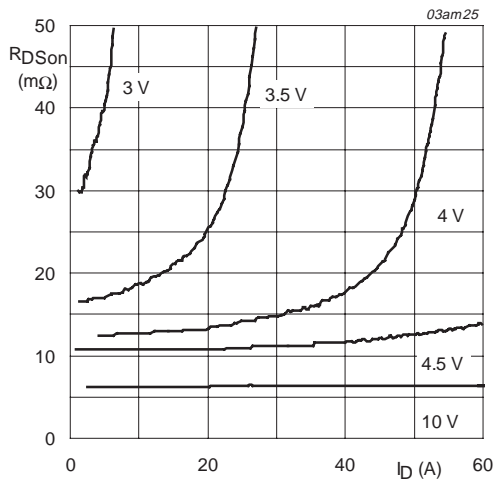
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



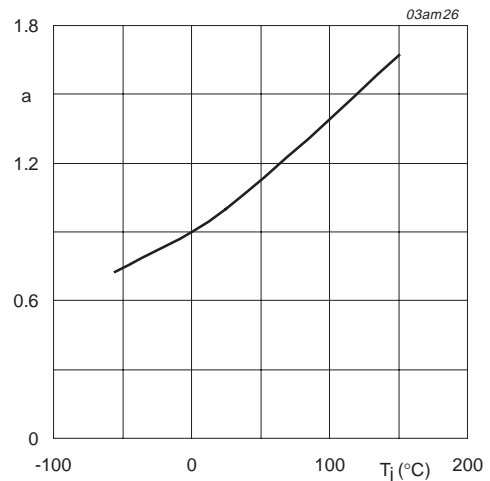
$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



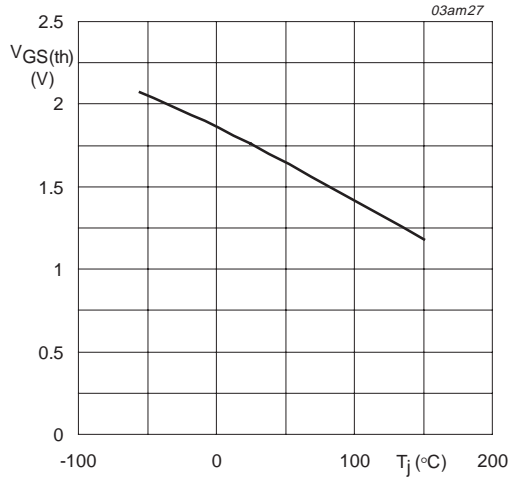
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



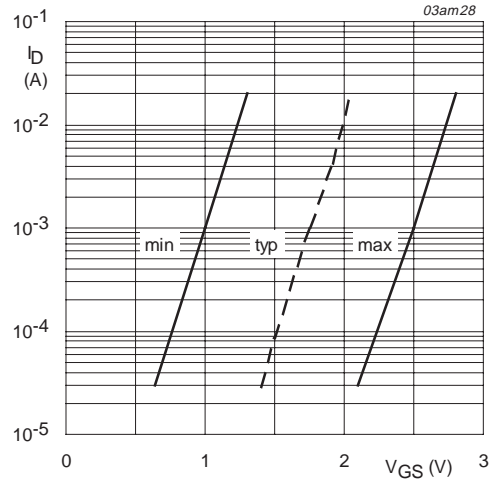
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



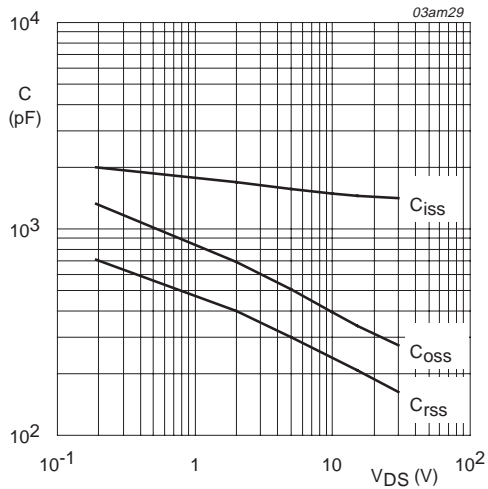
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



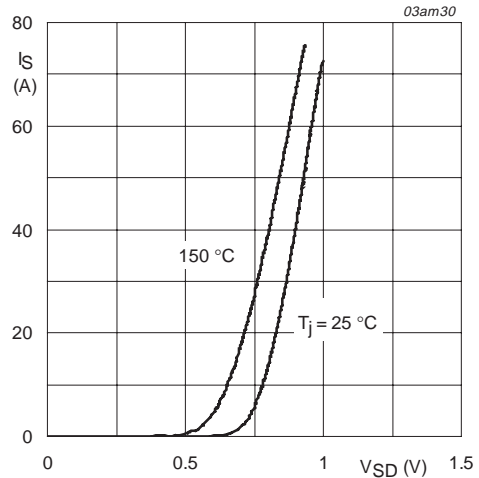
$T_j = 25 \text{ °C}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



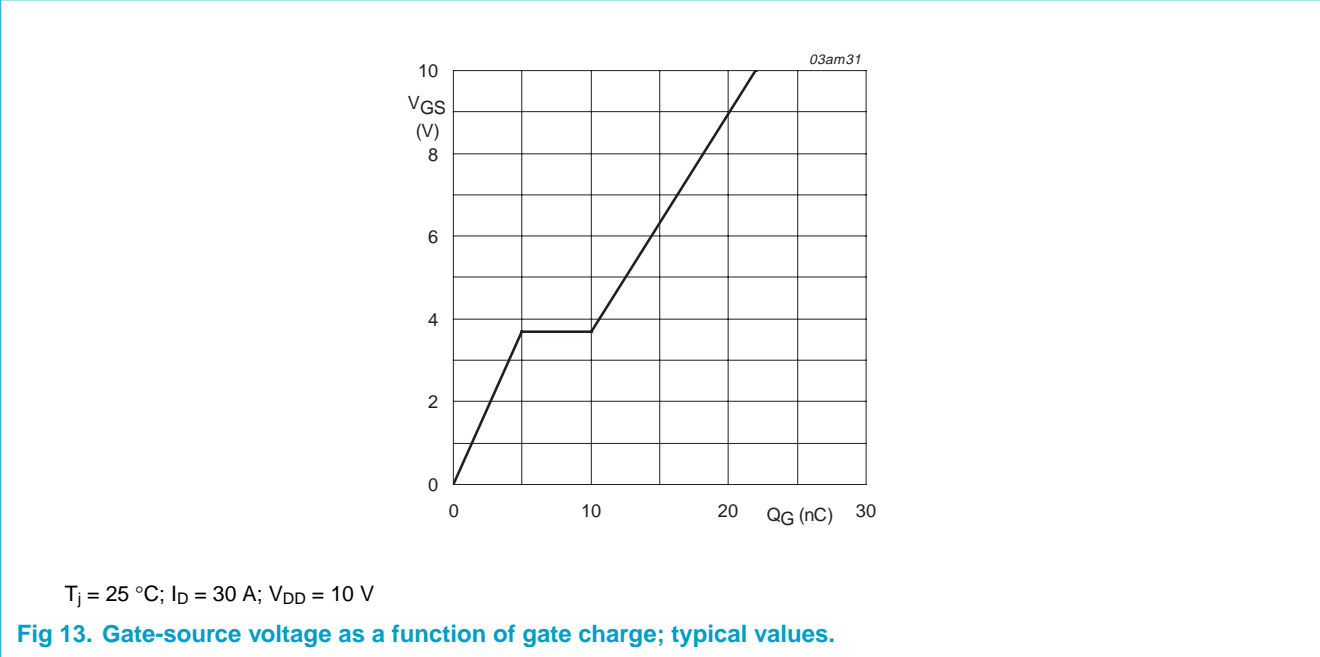
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25 \text{ °C and } 150 \text{ °C}; V_{GS} = 0 \text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



6. Package outline

Plastic single-ended surface mounted package (Philips version LPAK); 4 leads

SOT669

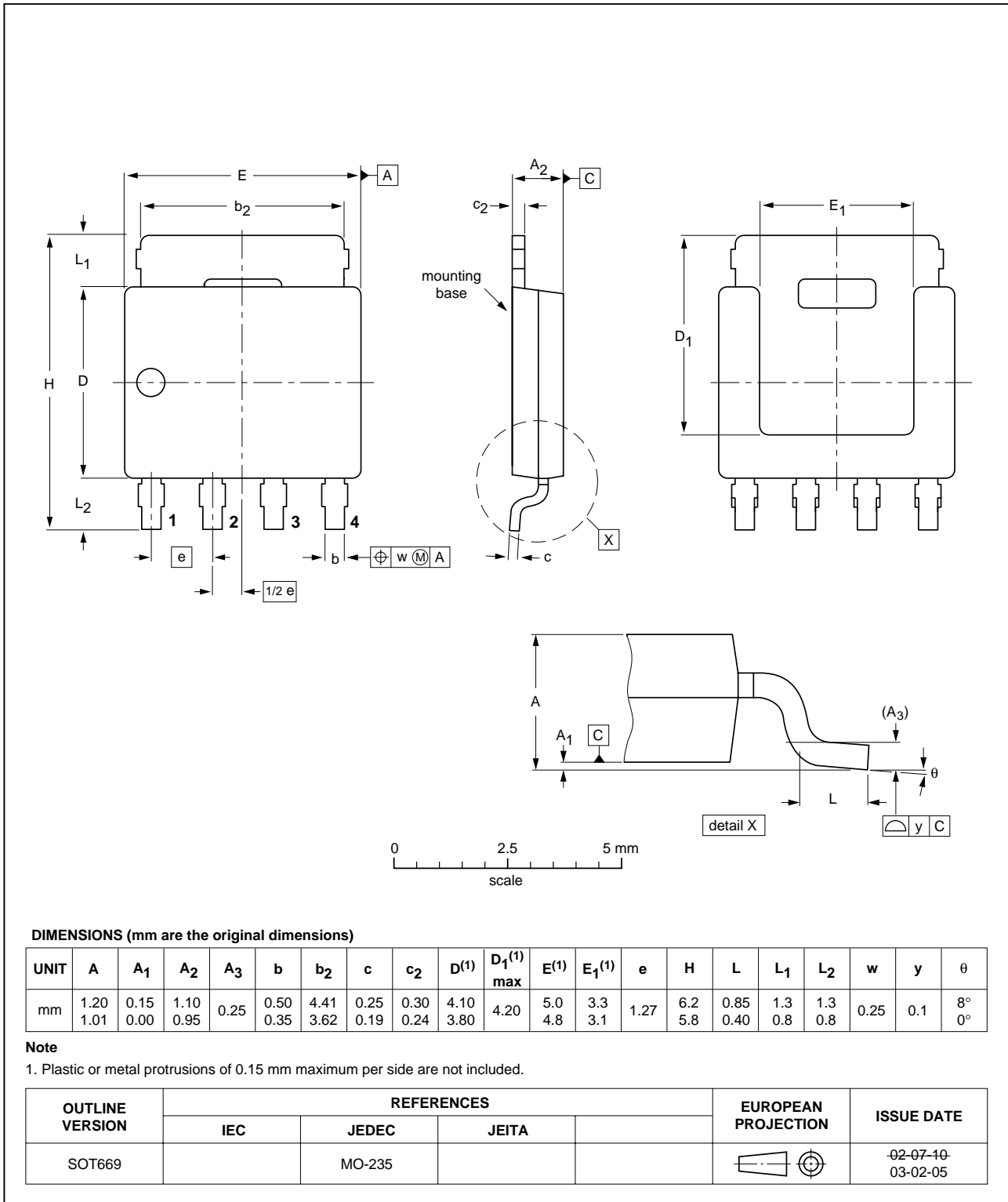


Fig 14. SOT669 (LPAK).

7. Revision history

Table 5: Revision history

Rev	Date	CPCN	Description
01	20030623	-	Product data (9397 750 11118)

8. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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